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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,302	10/09/2003	Makoto Kudo	105746.01	7992

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EXAMINER

YANCHUS III, PAUL B

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/681,302	Applicant(s) KUDO ET AL.	
	Examiner Paul B. Yanchus	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6-8 and 11 is/are rejected.
- 7) ☐ Claim(s) 4, 5, 8, 9, 14 and 15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/9/03</u> . | 6) <input type="checkbox"/> Other: _____ |

S. J. O.

DETAILED ACTION

Claim Objections

Claim 4 is objected to because of the following informalities: There appears to be a typographical error in line 4 of claim 4. The marking, “...” appears to have been included erroneously. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 6-8, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of, Katoozi et al., US Patent no. 5,594,631 [Katoozi].

Regarding claim 1, AAPA discloses a known PWM (pulse width modulation) control circuit for generating a PWM signal, comprising:

a counter for incrementing or decrementing a count value in accordance with a given operation clock [COUNTER in Figure 1B and page 1, lines 17-18];

an edge-point value setting register for storing an edge-point value which specifies a first edge-point at which the level of the PWM signal varies [EDGE-POINT VALUE SETTING REGISTER in Figure 1B and page 1, lines 18-22];

a PWM output circuit for varying the level of the PWM signal at said first edge-point specified by said edge-point value, based on said count value from said counter and said edge-point value from said edge-point value setting register [COMPARATOR (906) in Figure 1B and page 1, line 23 – page2, line 2]; and

a period value setting register for storing a period value which specifies a period of the PWM signal [PWM PERIOD VALUE SETTING REGISTER in Figure 1B and page 1, lines 15-17].

AAPA does not disclose using at least one bit on the low order side of the edge-point value as a delay value for delaying the edge-point by a period which is smaller than one clock period of the operation clock. Katoozi discloses a PWM control circuit similar to the AAPA PWM control circuit, but further discloses using at least one bit [LSB's of C'_e in Figure 5] on the low order side of the edge-point value [C'_e in Figure 5] as a delay value for delaying the edge-point by a period which is smaller than one clock period of the operation clock [column 8, lines 15-50]. It would have been obvious to one of ordinary skill in the art to incorporate the features of the Katoozi PWM control circuit in the AAPA PWM control circuit. One would be motivated to incorporate the features of the Katoozi PWM control circuit to provide a higher resolution in controlling the width of a control pulse without increasing the PWM clock frequency [Katoozi, column 3, lines 12-13 and column 8, lines 20-25].

Regarding claim 2, as described above, Katoozi discloses that the delay time is determined by the LSB's of the edge-point value [column 8, lines 40-43]. Katoozi further discloses that the delay time increments, N, are selectable, such that the period of each clock cycle is divided into N equal time increments [column 8, lines 26-35]. A value of 2 for N would set the delay time increment to one half of the clock cycle period.

Regarding claim 3, Katoozi further discloses:

a comparator for comparing said count value from said counter with said edge-point value from said edge-point value setting register to generate a first signal having a signal level which varies at said first edge-point specified by said edge-point value [DIGITAL COMPARATOR (72') in Figure 5 and column 7, lines 8-13];

a delay circuit for generating a second signal having a signal level which varies at a point delayed from said first edge-point by one-half clock period of said operation clock, based on said first signal and said operation clock [VERNIER in Figure 5 and column 8, lines 27-50; and

a multiplexer for selecting said first signal when said one-bit delay value stored in said delay value setting register is at a first level, and for selecting said second signal when said one-bit delay value is at a second level [MULTIPLEXOR in Figure 6 and column 8, lines 31-50].

Regarding claims 6-8, AAPA further discloses that known PWM control circuits are included in microcomputers, which inherently possess programmable timers [page 2, lines 10-12 and page 7, line 26 – page 8, line 1]. Katoozi discloses a processor for executing instructions and for performing processing for storing said edge-point and delay values in said edge-point and delay value setting registers in said PWM control circuit [DIGITAL SIGNAL PROCESSOR in Figure 3, Figure 5 and column 5, lines 33-40].

Regarding claims 11-13, AAPA further discloses that a known PWM control circuit may be used by an output sound device of a known game apparatus or car navigation system. A game apparatus and a car navigation system each inherently possess a source of input data to be processed.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoozi et al., US Patent no. 5,594,631 [Katoozi], in view of, Tocci, "Digital Systems Principles and Applications" [Tocci].

Regarding claim 1, Katoozi discloses a PWM (pulse width modulation) control circuit for generating a PWM signal, comprising:

- a counter for incrementing or decrementing a count value in accordance with a given operation clock [PULSE WIDTH COUNTER in Figure 5 and column 6, lines 58-59];

- an edge-point value which specifies a first edge-point at which the level of the PWM signal varies [C'_e in Figure 5 and column 6, lines 56-58 and column 7, lines 8-13];

- a PWM output circuit for varying the level of the PWM signal at said first edge-point specified by said edge-point value, based on said count value from said counter and said edge-point value [DIGITAL COMPARATOR (72') and VERNIER in Figure 5 and column 7, lines 8-13];

- a delay value, on low order side of said edge-point value, of at least one bit which specifies a delay time of said first edge-point [LSB's of C'_e in Figure 5 and column 8, lines 15-17 and 40-43]; and

a period value setting register for storing a period value which specifies a period of the PWM signal [FREQUENCY REGISTER in Figure 5 and column 6, line 65 – column 7, line 7],

wherein said PWM output circuit delays said first edge-point by a period which is smaller than one-clock period of said operation clock, in accordance with said delay value [column 8, lines 15-50].

Katoozi does not show registers for storing the edge-point value and delay value. However, as shown by Tocci, registers are commonly used in digital systems to store data or to assist in transmitting data from one location to another [paragraph 2 on page 330]. It would have been obvious to one of ordinary skill in the art to include well known registers in the Katoozi system to ensure that the edge point and delay values are not inadvertently lost when being transferred from the Signal Processor [See Figure 5] to the Digital Comparator and the Vernier.

Claims 6-8 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoozi et al., US Patent no. 5,594,631 [Katoozi] and Tocci, "Digital Systems Principles and Applications" [Tocci], in view of, Applicant's Admitted Prior Art [AAPA].

Regarding claims 6-8, Katoozi discloses a processor for executing instructions and for performing processing for storing said edge-point and delay values in said edge-point and delay value setting registers in said PWM control circuit [DIGITAL SIGNAL PROCESSOR in Figure 3, Figure 5 and column 5, lines 33-40]. Katoozi does not indicate the PWM control circuit is used in microcomputers with programmable timers. AAPA discloses that known PWM control circuits are included in microcomputers, which inherently possess programmable timers [page 2, lines 10-12 and page 7, line 26 – page 8, line 1]. It would have been obvious to one of ordinary

Art Unit: 2116

skill in the art to include the Katoozu and Tocci PWM control circuit into known microcomputers to assist in the operation of a programmable timer.

Regarding claims 11-13, AAPA further discloses that a known PWM control circuit is used by an output sound device of a known game apparatus or car navigation system. A game apparatus and a car navigation system each inherently possess a source of input data to be processed.

Allowable Subject Matter

Claims 4, 5, 9, 10, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2116

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
June 2, 2005



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SUPERVISORY PATENT EXAMINER
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